

IN THE CLAIMS:

1-20. (Currently Canceled)

21. (Original) A method for fabricating a memory array having a plurality of memory cells, the method comprising the steps of:
providing a wafer having at least one silicon carbide (SiC) layer; and
fabricating each of the plurality of memory cells over the at least one SiC layer.

22. (Original) The method according to Claim 21, wherein the plurality of memory cells are a plurality of T-RAM memory cells

23. (Original) The method according to Claim 22, wherein each of the plurality of T-RAM cells has a size of less than or equal to $6F^2$.

24. (Original) The method according to Claim 22, wherein each of the plurality of T-RAM memory cells includes a first portion and a second portion.

25. (Original) The method according to Claim 24, wherein the first portion is a thyristor and the second portion is a transfer gate.

26. (Original) The method according to Claim 21, further comprising the step of encapsulating each of the plurality of memory cells with an insulating material.

27. (Original) The method according to Claim 21, further comprising the step of fabricating each of the plurality of memory cells with a planar cell structure.

28. (Original) The method according to Claim 21, further comprising the step of providing three layers on the wafer prior to the fabricating step, wherein a first layer is provided on top of the at least one SiC layer and is an n-type layer, a second layer is provided on top of the first layer and is a p-type layer, and a third layer is provided on top of the second layer and is an n-type layer.

29. (Original) The method according to Claim 21, wherein the step of fabricating each of the plurality of memory cells on the wafer includes the steps of:

doping portions of the wafer with a first doping implant; and

doping portions of the wafer in proximity to the portions doped with the first doping implant with a second doping implant.

30. (Currently Amended) The method according to Claim 29, wherein the first doping implants is a p-type doping implant and the second doping implant is an n-type doping implant.

31. (Original) The method according to Claim 29, wherein the step of doping portions of the wafer with a first doping implant includes the step of using a p-type boron implant at an energy in the range of 0.5 to 2 KeV and a dosage of between 2E14/cm² and 8E14/cm² as the first doping implant.

32. (Original) The method according to Claim 29, wherein the step of doping portions of the wafer with a second doping implant includes the step of using an n-type arsenic implant at an energy in the range of 2 to 15 KeV and a dosage of between 8E14/cm² and 3E15/cm² as the second doping implant.

33. (Currently Amended) The method according to Claim 21, wherein the wafer includes a first layer formed by implanting an n+ type arsenic implant at an energy in the range of 2 to 15 KeV and a dosage of between 8E14/cm² to 3E15/cm²; a second layer formed by epitaxial growth using p-type boron at a dosage of between 4E13/cm² to 1E14/cm²; and a third layer formed by epitaxial growth using n- type arsenic at a dosage of between 2E13/cm² to 8E13/cm².

34. (Original) The method according to Claim 29, further comprising the steps of:

providing a first mask to conceal the portions of the wafer doped with the first and second doping implants;

etching portions of a first layer of the wafer which are not concealed by the first mask;

removing the first mask and depositing a dielectric layer over the wafer; and
providing a second mask and etching portions of a second layer of the wafer which are
not concealed by the second mask.

35. (Original) The method according to Claim 34, further comprising the steps of:
etching portions of a third layer of the wafer in alignment with the etched portions of the
second layer;
forming a gate dielectric layer on the wafer and depositing a semiconductor material to
form a semiconductor layer over the gate dielectric layer;
providing a third mask and etching portions of the semiconductor layer and the gate
dielectric layer which are not concealed by the third mask; and
removing the third mask and etching portions of the second layer of the wafer and the
dielectric layer which are not in vertical alignment with the semiconductor layer.

36. (Original) The method according to Claim 35, further comprising the steps of:
oxidizing surfaces which are not in vertical alignment with the semiconductor layer;
providing a fourth mask and etching portions of the oxidized surfaces and the third layer
of the wafer which are not concealed by the fourth mask to define first and second portions of
each of the plurality of memory cells;
providing a vertically aligned contact in the first and second portions of each of the
plurality of memory cells; and
adding an insulating material to encapsulate the first and second portions of each of the
plurality of memory cells and to provide a planar structure for the array.

37. (Original) The method according to Claim 36, further comprising the steps of:
forming a plurality of bitlines traversing the plurality of memory cells; and

forming a plurality of voltage reference lines traversing the plurality of memory cells.

38. (Original) The method according to Claim 21, wherein the at least one SiC layer is a p-type layer.

39. (Original) The method according to Claim 21, wherein each of the plurality of memory cells is configured for being operational at high temperatures and in high radiation prone environments.

40. (Original) The method according to Claim 39, wherein each of the plurality of memory cells is operational in a temperature range from 200 to 1000 degrees Celsius.